IN THE CLAIMS:

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) A thin film transistor ~~according to claim 3, wherein~~ comprising:

a polycrystalline silicon semiconductor layer having therein a channel region, a source region, and a drain region, the source region and the drain region located on either side of the channel region, the drain region including a lightly doped drain (LDD) region; and

wherein the relationship of expression (2)

$$(R+30)\cdot W<1\times10^{3} \qquad (2)$$

is satisfied, where R (kΩ/□) is the sheet resistance of the LDD region and W (μm) is the channel width of the channel region, the channel width W of the channel region ~~is~~ being 2 μm or less.

5. (Cancelled)

6. (Currently Amended) A thin film transistor according to claim 4, wherein the sheet resistance of the ~~drain~~ LDD region in the range of from 20 kΩ/□ to 100 kΩ/□.

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7. (Cancelled)

8. (Currently Amended) A thin film transistor comprising a polycrystalline silicon semiconductor layer having ~~formed~~ therein a channel region, a source region, a drain region, and a low concentration impurity region having an impurity concentration less than that of the source region and the drain region, the source region and the drain region being ~~disposed~~ located on either side of the channel region and the low concentration impurity region being ~~formed~~ located in at least one of a region between the source region and the channel region and a region between the drain region and the channel region, the thin film transistor wherein:

the relationship of expression (3)

$$\Delta L > (W \cdot Vlc)/36 \qquad (3)$$

is satisfied, where ΔL (μm) is the length of the low concentration impurity region, Vlc (V) is the source-drain voltage, and W (μm) is the channel width of the channel region, the channel width W (μm) of the channel region being 2 μm or less.

9. **(Currently Amended) A thin film transistor** ~~according to claim 8, wherein~~ comprising a polycrystalline silicon semiconductor layer having therein a channel region, a source region, a drain region, and a low concentration impurity region having an impurity concentration less than that of the source region and the drain region, the source region and the drain region being located on either side of the channel region and the low concentration impurity region being located in at least one of the region between the source region and the channel region and a region between the drain region and the channel region, the thin film transistor wherein:

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the relationship of expression (4)

$$\Delta L < 1.5 \cdot (W / L) \qquad \textbf{(4)}$$

is satisfied, where ΔL (μm) is the length of the low concentration impurity region, W (μm) is the channel width of the channel region, and **L (μm) is the**

channel length of the channel region, the channel width W (μm) of the channel region being 2 μm or less.

10. **(Currently Amended) A thin film transistor** ~~according to claim 9, wherein~~ comprising a polycrystalline silicon semiconductor layer having therein a channel region, a source region, a drain region, and a low concentration impurity region having an impurity concentration less than that of the source region and the drain region, the source region and the drain region being located on either side of the channel region and the low concentration impurity region being located in at least one of the region between the source region and the channel region and a region between the drain region and the channel region, the thin film transistor wherein:

the relationship of expression (20)

$$(W-Vlc)/36<\Delta L<1.5\cdot(W/L) \qquad (20)$$

is satisfied, wherein ΔL (μm) is the length of the low concentration impurity region, Vlc (V) is the source-drain voltage, W (μm) is the channel length of the channel region, **the channel width W (μm) of the channel region ~~is~~ being 2 μm or less.**

11. (Currently Amended) A thin film transistor ~~according to claim 9~~ comprising a polycrystalline silicon semiconductor layer having therein a channel region, a source region, a drain region, and a low concentration impurity region having an impurity concentration less than that of the source region and the drain region, the source region and the drain region being located on either side of the channel region and the low concentration impurity region being located in at least one of a region between the source region and the channel region and a region between the drain region and the channel region, the thin film transistor wherein:

the relationship of expression (3)

$$\Delta L > (W \cdot Vlc)/36 \qquad (3)$$

is satisfied, where ΔL (μm) is the length of the low concentration impurity region, Vlc (V) is the

source-drain voltage, and W (μm) is the channel width of the channel region, the channel width W (μm) of the channel region being 2 μm or less, **wherein the sheet resistance of the low concentration impurity region is in the range of from 20 kΩ/□ to 100 kΩ/□.**

12. (Cancelled)

14

13. (Original) A thin film transistor according to claim 11, wherein the low concentration impurity region is formed only in the region between the drain region and the channel region.

14. (Cancelled)

15. (Currently Amended) A liquid crystal display device ~~according to claim 14~~ comprising:

a liquid crystal panel portion comprising thin film transistor switching elements, each of the thin film transistors having a polycrystalline silicon semiconductor layer having therein a channel region,

a source region, and a drain region, the source region and the drain region located on either side of the chanel region, the drain region having located therein a lightly doped drain (LDD) region; and

a backlight portion for supplying light from a rear surface side of the liquid crystal panel portion;

wherein the relationship of expression (6)

$$(R+30)\cdot B\cdot W<1\times10^{6} \qquad (6)$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the luminance of the backlight portion, and W (μm) is the channel width of the channel region, the channel width W being 2 μm or less.

16. (Cancelled)

17. (Currently Amended) An EL display device ~~according to claim 16,~~ comprising a light-emitting layer and a counter electrode thereon, the light-emitting layer being on a pixel

electrode upper layer on a substrate having thin film transistors, each of the thin film transistors comprising:

a polycrystalline silicon semiconductor layer having therein a channel region, a source region, and a drain region, the source region and the drain region located on either side of the channel region, the drain region having located therein a lightly doped drain (LDD) region; and

wherein the relationship of the expression (6)

$$(R+30)\cdot B\cdot W<1\times10^{6} \qquad (6)$$

is satisfied, where R (kΩ/□) is the sheet resistance of the ~~drain~~ LDD region, B (cd/m^2) is the light intensity of light applied to the channel region, and W (μm) is the channel width of the channel region, the channel width W being 2 μm or less.

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (New) A thin film transistor comprising a polycrystalline silicon semiconductor layer having therein a channel region, a source region, a drain region, and a low concentration impurity region having an impurity concentration less than that of the source region and the drain region, the source region and the drain region being located on either side of the channel region and the low concentration impurity region being located in at least one of the region between the source region and the channel region and a region between the drain region and the channel region, the thin film transistor wherein:

the relationship of expression (4)

$$\Delta L < 1.5 \cdot (W / L) \qquad (4)$$

is satisfied, where ΔL (μm) is the length of the low concentration impurity region, W (μm) is the channel width of the channel region, and L (μm) is the channel length of the channel region, the channel width W (μm) of the channel region being 2 μm or less, wherein the sheet resistance of the low concentration impurity region is in the range of from 20 kΩ/□ to 100 kΩ/□.

22. (New) A thin film transistor comprising a polycrystalline silicon semiconductor layer having therein a channel region, a source region, a drain region, and a low concentration impurity region having an impurity concentration less than that of the source region and the drain region, the source region and the drain region being located on either side of the channel region and the low concentration impurity region being located in at least one of the region between the source region and the channel region and a region between the drain region and the channel region, the thin film transistor wherein:

the relationship of expression (20)

$$(W-Vlc)/36<\Delta L<1.5\cdot(W/L) \qquad (20)$$

is satisfied, wherein ΔL (μm) is the length of the low concentration impurity region, Vlc (V) is the source-drain voltage, W (μm) is the channel length of the channel region, the channel width W (μm) of the channel region being 2 μm or less, wherein the sheet resistance of the low concentration impurity region is in the range of from 20 kΩ/□ to 100 kΩ/□.